Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 10, and 21 have been amended. No claims have been cancelled or added. Therefore, claims 1-30 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1-30 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Sih et al. (U.S. Patent No. 6,606,700). Applicant submits that the present claims are patentable over Sih.

Sih discloses a digital signal processor architecture that is designed to speed up frequently-used signal processing computations, such as FIR filters, correlations, FFTs, and DFTs. The architecture uses a coupled dual-MAC architecture and attaches a dual-MAC coprocessor onto it in such a way as to achieve an increase in processor capability. (Sih at col. 1, ll. 49-55.)

Claim 1, as amended, recites:

> A method comprising:
> receiving input data by an execution unit; and
> performing by the execution unit using one or more multiply-accumulate units in the execution unit one or more current multiply-accumulate operations on the received input data and on input data received by the execution unit for one or more prior multiply-accumulate operations and saved by the execution unit;
> wherein the performing one or more current multiply-accumulate operations includes:
> multiplying one or more input values with a multiplier in the execution unit;
> adding an output from the multiplier with another value using an adder in the execution unit; and

storing an output of the adder and providing the another value to the adder using an accumulator in the execution unit.

Applicant submits that Sih does not disclose or suggest performing a multiply-accumulate operation in each multiply-accumulate unit by storing an output of an adder and providing another value to the adder using an accumulator in the execution unit. The multiply-accumulate (MAC) units of Sih do not disclose the accumulator in *each MAC* performing accumulation by using their own accumulator results. Instead, two of the MACs in Sih must perform accumulation by "fetching and storing results to [a] register file" that is not located within the MAC unit. (Col. 4, ll. 44-48.) Therefore, claim 1 is patentable over Sih.

Claims 2-9 depend from claim 1 and include additional limitations. Therefore, claims 2-9 are also patentable over Sih.

Independent claims 10 and 21 also recite, in part, each multiplier-accumulator including a multiplier to multiply one or more input values, an adder to add an output from the multiplier with another value, and an accumulator to store an output from the adder and provide the another value to the adder. As discussed above, Sih does not disclose or suggest such a feature. Therefore, claims 10 and 21 are patentable over Sih for the reasons discussed above with respect to claim 1. Claims 11-20 and 22-30 depend from claims 10 and 21, respectively, and include additional limitations. Therefore, claims 11-20 and 22-30 are also patentable over Sih.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

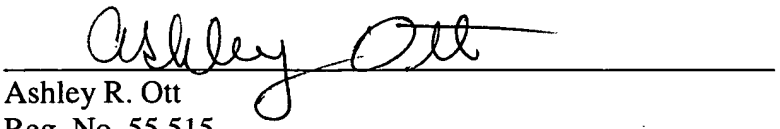
Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: May 24, 2005



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